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2	BRS	L2	8	1 and eras\$3 and (bulk or substrate) and (voltage or charge	USPAT	2003/05/04
				or bias or potential) and time and gate and greater and	US-PG	
				impurity	US-PG	
3	BRS	L3	29	1 and eras\$3 and (bulk or substrate) and (voltage or charge	USPAT	2003/05/04
				or bias or potential) and time and gate and greater	US-PG	

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or approximately 2 to 5 V is applied to the source so that essentially no current will flow from the source to the substrate. In addition, the control gate is also appropriately biased so that there will be essentially no flow of channel current either. When a reverse bias of approximately 14 V is then applied between the drain and substrate, a current-avalanche effect is produced in the vicinity of the drain junction beneath the gate oxide film. This avalanche comprises for example hot positive-carrier holes which in turn become injected into the floating gate, thereby neutralizing the previously channel-injected opposite-carrier charge.

More specifically, as shown in FIG. 6a, the switch I is first closed and the switch II is opened, so that  $V_G = V_B = 0$  V and  $V_S = 2$  V are applied to the cell. Next, as shown in FIG. 6b, the switch II is closed, and a pulse of  $V_D = 14$  V is applied to the drain 42, thereby effecting erasure. Thus by appropriate alterations in applied voltages, not only the writing of data but also the erasing of data can be accomplished electrically.

FIG. 7 shows the relationship between applied erase-pulse duration-time  $T_E$  and resultant  $V_T$  under these conditions. It is seen from FIG. 7 that in the case of a cell in which  $V_{TA}$  is 6.6 V, the value of  $V_T$  drops to 2.0 V after a 50-msec application, so that the cell almost returned to its original, pre-writing state. After approximately this 50 msec, moreover, the erasure curve becomes essentially asymptotic.

o, the drain voltage  $V_D$  breakdown occurs increased from 1 V to 3 V biasing of the source with it possible to maintain the location which contributes the occurrence of breakdown result in the flow of an e

It may be noted parenthetically that the only way of avoiding breakdown. This objective is achieved by biasing the substrate  $V_B$  even if the source potential is floating, the subject source potential during the pulse between the source and the substrate accordingly be the same as the source biasing.

FIG. 9 next shows the characteristics with the source potential. Here, the floating gate potential is a parameter, and the substrate potential is another parameter. Figure 9 shows that avalanche occurs at lower drain voltages as the floating gate potential  $V_{FG}$  drops. This is that the electric field at the drain junction increases as the floating gate potential  $V_{FG}$  drops.